



## Simplifying software systems through modular design

Lynx MOSA.ic™ is a software development framework for rapidly building comprehensible software systems out of independent application modules, delivering the vision of the Modular Open Systems Approach (MOSA). Its focus is to enable developers to collapse existing development cycles to create, certify, and deploy robust, secure platforms for manned and unmanned autonomous systems. It achieves this by giving developers deeper insight.

Traditional approaches to creating a virtualized embedded software architecture have placed much of the burden in a hypervisor and/or operating system. This can create platform dependencies which have an impact on performance due to extra copies and context switches, as well as causing a number of architecture challenges due to:

- Shared address space
- Shared CPU privilege
- Common arbitration points
- Global resource pools
- Compounding code branches
- Compounding control flow timing
- Large co-dependent code base to certify

In contrast to a traditional RTOS platform, where all hardware control, real-time scheduling, security, multimedia, and application runtime services are integrated into a common stack, servicing all applications on all CPU cores, LYNX MOSA.ic

allows system architects to subdivide systems into smaller, independent stacks. The benefits of stack separation yield program value from software complexity reduction by in software complexity by:

- Promoting traceable, comprehensible architectures
- Giving evaluators the ability to truly validate security and safety properties
- Reducing time to debug
- Increasing the speed of system integration

### Clearer path to multi-core certification

Lynx MOSA.ic™ adapts to the advances in multi-core virtualization to simplify vital platform abstraction layers. The hardware enforced architecture of Lynx MOSA.ic™ makes inherently complex, multi-core system development a viable option for building solutions in highly regulated safety- and security-conscious markets.

The Framework is comprised of three distinct classes of tools  
Architecture Design, Module Development, & System Module Integration.

### Module development & system module integration

A cross development kit is included for building guests of varying size, quality, and complexity specific to their target environments. Integration tools connect legacy, competitor, or partner-provided guests together.

#### Lynx CDK guest support

- Lynx Simple Application (Bare Metal Application)
- LSA.store – Bare-Metal Crypto Module XTS-AES 256
- Z-Scheduling – Real-time scheduling
- Guest IPC – Point-to-Point FIFO
- Debug – Lauterbach TRACE 32 Integration

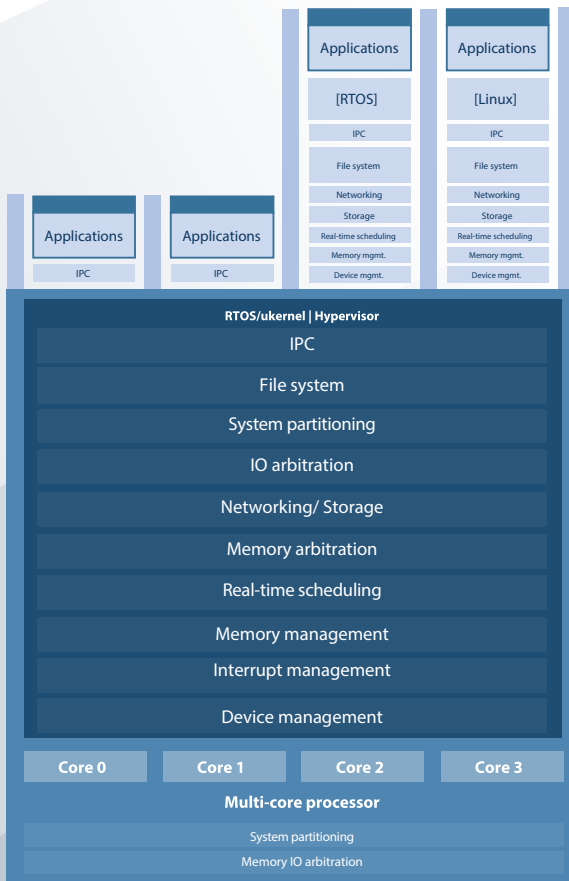
### Architecture design

- Bare-metal – Raw 64-bit guest contexts
- RTOS – Lightweight context support for real-time scheduling and certified code bases
- Legacy OS – Hardware emulation support for legacy code bases

Communication channels—Explicit point-to-point memory regions link VMs together via standard IPC interfaces, maximizing performance and ensuring minimal complexity.



- LynxOS-178**
  - UNIX-like Real Time Operating System
  - Certs – DO 178 DAL A, FAA Reusable Software Component
  - APIs – POSIX, FACE, ARINC 653
  - Scheduling – Priority Pre-emptive, Cyclic
  - Debug – Lauterbach TRACE 32, Eclipse IDE Profiling & GDB
  - Guest IPC – Point-to-Point FIFO, Ethernet UART
- Buildroot**
  - Embedded Linux Toolchain
  - APIs – POSIX, FACE
  - Guest IPC – Point-to-Point FIFO, Ethernet, UART
  - Device Sharing (Intel) – SRIOV, GFX, USB, Storage, Ethernet
  - Debug – Eclipse IDE GDB
- Types**
  - FIFO • Ethernet • Device Emulation

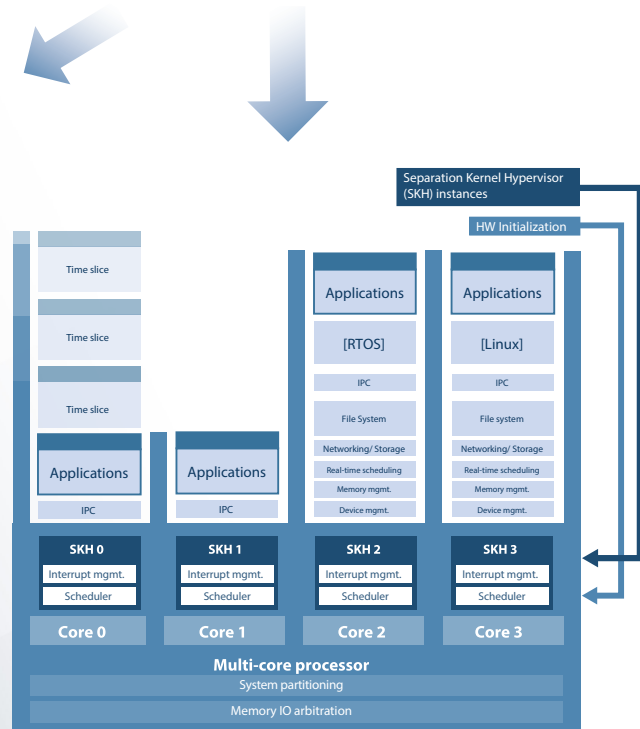
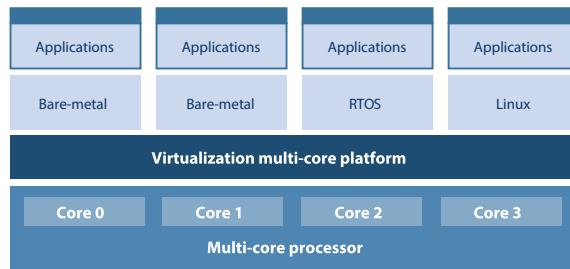


**Traditional RTOS + hypervisor platforms**

### Processor partitioning system

Processor resources are partitioned with an architecture configuration policy to control the behavior of the system. Enforce the policy with a least privilege distributed control plane that creates VMs and communication channels for guests.

- Processors**
  - Arm v8-A
  - Intel VTx
  - Power PC



**Separation kernel hypervisor**



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